REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority under 35 U.S.C. § 119(a)-(d), and for confirming that the certified copy of the priority document has been received at the Patent Office in U.S. Application No.: 10/357,494.

Drawings:

Applicant thanks the Examiner for indicating that the drawings filed on June 28, 2004 have been approved.

Information Disclosure Statement:

Applicant thanks the Examiner for initialing and returning Form PTO/SB/08 A & B filed on March 26, 2004 and June 28, 2004, thus indicating that all of the references listed thereon have been considered.

Claim Rejections:

Claims 1, 11, 12, 14 and 15 are all of the claims that have been examined in the present application, and currently all of these claims have been rejected.

Applicant has canceled claims 1 and 12 without prejudice or disclaimer.

35 U.S.C. § 112, 2nd Paragraph Rejection - Claims 11 and 14-15:

Claims 11 and 14-15 stand rejected under 35 U.S.C. § 112, 2nd paragraph as being indefinite. Specifically, the Examiner has indicated that there are a number of portions of these claims which render them unclear to a skilled artisan.

Applicant has amended each of claims 11, 14 and 15 as shown in the previous section and hereby submits that these amendments address the Examiner's concerns regarding these

claims. Specifically, Applicant submits that these claims are clear and definite to a person of ordinary skill in the art.

With regard to claims 1 and 15, Applicant is unclear as to what the Examiner meant when the Examiner indicated that "the initial serial data pulse was defined as having 'a resolution lower than a resolution needed by the serial video data' and would not be acceptable as serial data pulse." Office Action, page 2, last paragraph; and page 3, last paragraph. However, in any event, Applicant has amended both claims 1 and 15 as shown in the previous section to address the Examiner's concerns. Further, Applicant submits that the scope of both of these claims are clear and definite to a skilled artisan. Support for the amendment to these claims can be found at, at least, page 37, lines 4-6; page 40, lines 2-4; page 39, line 14 to page 40, line 4; and Figures 3-11, of the present application.

In view of the foregoing, Applicant hereby requests the Examiner reconsider and withdraw the above 35 U.S.C. § 112, 2nd paragraph rejection of these claims.

Further, Applicant notes that the above referenced claim amendments have been made to merely clarify the claimed invention and are not intended to narrow the original scope or spirit of the claims in any way.

35 U.S.C. § 103(a) Rejection - Claims 11 and 14-15:

Claims 11 and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,335,696 to Aoyagi et al. in view of U.S. Patent No. 4,165,490 to Howe Jr. et al. In view of the following discussion, Applicant respectfully traverses the above rejection.

In rejecting the claims, the Examiner insists that Aoyagi discloses, *inter alia*, both the "n-stage clock signal delaying unit" and the "n-stage delayed pulse gate" of the claimed invention. For at least the following three reasons, Applicant respectfully disagrees with the Examiner.

First, the "n-stage clock signal delaying unit" of the claimed invention contains a plurality of signal delay devices placed in a predetermined clock signal line. *See* claim 11. A non-limiting example of a signal delay device is the buffer 520a, shown in Figure 13. Applicant submits that this is neither disclosed or suggested in either of the above cited references. Namely, Aoyagi discloses using a "tap signal generator 10." The tap signal generator is a DLL (Delayed Lock Loop, *see* Aoyagi, column 2, line 47). It is understood by those of ordinary skill in the art that a DLL needs complicated circuitry to lock a desirable delay time. A tap signal generator does not employ a plurality of signal delay devices placed in a predetermined clock signal line. Thus, by using Aoyagi a skilled artisan would be unable to obtain a delayed-pulse with simple circuitry, as is achieved with the present invention. Accordingly, even if the references were combined, the resultant combination would fail to teach or suggest each and every feature of the claimed invention.

Secondly, Aoyagi fails to teach or suggest the "delayed pulse input unit" of the claimed invention. *See* claim 11. In the claimed invention, the "delayed pulse input unit" applies the delayed pulse passed the "nth delayed pulse gate" to a clock signal line of an "(n+1)th clock signal delaying unit". Claim 11. Thus, in the present invention, because an output of the n-stage delayed pulse gate (nth delayed pulse gate) is applied to the (n+1)-stage clock signal delaying unit ((n+l)th clock signal delaying unit), n+1 pieces of circuits are repeated. A non-limiting example of this is shown in at least Figure 13 of the present application. However, this is neither

taught or suggested in Aoyagi. In fact, in Aoyagi the "tap signal generator 10" and "selection signal generator 11" lack the repeating of circuitry, as set forth above in the claimed invention. Therefore, again, even if the references were combined, the resultant combination would fail to teach or suggest each and every feature of the claimed invention.

Finally, Aoyagi lacks "an n-stage delayed pulse gate" as set forth in the claimed invention. Specifically, the "n-stage delayed pulse gate" passes a delayed pulse of time specified by the timing unit by a timing signal specifying the time of the delayed pulse. This is not disclosed in Aoyagi. Specifically, in Aoyagi, the "selection signal generator 11" does not simply pass a delayed pulse. Namely, the "selection signal generator 11" generates pulse signals SEL[0:9] from tap signal TAP[0:9] (Aoyagi, column 3, line 27), and the pulse width of SEL[0:9] differs from the pulse width of TAP[0:9] (Aoyagi, Fig. 4). Thus, Aoyagi fails to teach or suggest the "n-stage delayed pulse gate" of the present invention.

Because of the foregoing, the present invention is capable of obtaining a fine adjustment of a pulse edge. Namely, this capability is a result, at least in part, of the combination of the "n-stage clock signal delaying unit," the "n-stage delayed pulse gate," and the "delayed pulse input unit" as set forth and claimed in the present application. A non-limiting exemplary embodiment of this is shown in Figure 13, of the present application. The circuit shown in this Figure enables the fine adjustment of Figure 14, because the selection of HSCLKSET1[0] - HSCLKSET1[5] (Fig.13) corresponds to the selection of edge timings of a simply passed delayed pulse. This enables a fine adjustment of the edge of HSCLK1. This can be further seen in Fig. 14B, of the present application. Furthermore, because of the repeating of a circuit, a fine adjustment of

HSCLK2 and HSCLK3 is also possible. With the above elements, it is possible to adjust the edge timing around 1/4, 2/4, and 3/4 of half the period.

However, the combination of the "tap signal generator 10" and the "selection signal generator 11" disclosed by Aoyagi can never obtain adjustable plurality of delayed pulses around 1/4, 2/4, and 3/4 of half the period, because Aoyagi does not disclose the simple passing of the pulse and the repeating of the circuit, as in the present invention.

Finally, the Examiner asserts that Howe discloses the "coarse adjustment unit" and the "fine adjustment unit" of the claimed invention. However, as Howe suffers from the same deficiencies as Aoyagi, and also lacks the repeating of the circuit, Howe fails to cure the deficient teachings of Aoyagi. Therefore, Applicant provides herewith no independent discussion of the Howe reference.

In view of the foregoing, Applicant submits that Even if the references were combined, as suggested by the Examiner, the resultant combination would fail to teach or suggest each and every feature of the claimed invention. Therefore, Applicant submits that the Examiner has failed to establish a *prima facie* case of obviousness with respect to these claims, as required under the provisions of 35 U.S.C. § 103(a). Accordingly, Applicant hereby requests the Examiner reconsider and withdraw the above 35 U.S.C. § 103(a) rejection of the above claims.

Conclusion:

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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